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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,644	11/18/2003	Akira Sakai	117787	2533

25944 7590 10/31/2005

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EXAMINER	
DANG, TRUNG Q	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,644	SAKAI ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/16/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 8-11, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Toru et al. (JP-A-10-256169 with machined English translation submitted by applicants on 6/16/05).

With reference to Fig. 1b, the prior art teaches the claimed invention in that it discloses a method (first embodiment) for fabricating a SiGe film, comprising the steps of:

preparing a Si substrate 12;

forming a SiGe film 13 over said Si substrate; and

heat treating the resulting structure to form edge dislocations 16 at a bottom region of said SiGe film adjacent to an interface of said SiGe film and said Si substrate.

Note that although the English Abstract discloses that the epitaxial layer 13 is of Ge, the reference also includes the epitaxial layer 13 is of SiGe deposited on the Si substrate (see paras. [0011] and [0050]). Furthermore, the edge dislocation 16 is a 90

degrees dislocation because the Burger vector is perpendicular to the dislocation line (see Abstract).

For claims 2-4, the third embodiment disclosed at paragraph [0010] teaches a process comprises:

epitaxially growing a first Ge film on a silicon substrate;

forming a first capping layer (enveloping layer) of Si or SiGe on the first Ge film;

performing a first heat treatment on the resulting structure;

epitaxially growing a second Ge film on the first capping layer;

forming a second capping layer of Si or SiGe on the second Ge film;

performing a second heat treatment.

Note that the second Ge film can be a second SiGe as noted in paragraphs [0011] and [0050]. In this case, the first Ge reads on the claimed interfacial layer, the first SiGe capping layer reads on the claimed SiGe intermediate layer, and the second SiGe reads on the claimed SiGe film that is formed over the Si substrate. It is also noted that the heat treatment induces the edge dislocation in the semiconductor layer covered by the capping layer as described in the first embodiment, therefore the second heat treatment of the third embodiment would inherently induce the edge dislocation in the second SiGe layer, absent evident to the contrary.

For claims 8-11, the process described in the first and third embodiments would result in the structure as claimed.

For claim 15, see para. [0039] for the deposition of a silicon film on the substrate.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toru et al. as above.

Toru teaches a process and structure as noted above, including the step of forming the interfacial layer of Ge. Toru differs from the claims in that the thickness of the Ge interfacial layer is 20nm (para. [0021]) rather than 0.1-10nm as claimed. However, the determination of thickness values for the interfacial layer within the claimed range would have been obvious to one skilled in the art because it is well settle that, absent a showing of criticality or unexpected result by applicant, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ

809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d (Fed.cir), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed thickness range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in the claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d, 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

5. Claims 6-7 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toru et al. as above in view of Takasaki (US 5,188,778 of record).

Toru teaches a method and a structure as noted above. Toru differs from the claims in not disclosing a GaAs as an interfacial layer formed between the Si substrate and the SiGe layer. However, Takasaki teaches that the lattice constant of GaAs and Ge (or SiGe) are close to each other, hence defects are rarely generated at the interface between the two layers (col. 2, lines 35-39 and lines 48-49). Thus, the formation of a GaAs layer between the Si substrate 12 and the SiGe layer 13 would have been obvious to one of ordinary skill in the art because one skilled in the art would reasonably expected to achieve the same result for the reason that the lattice constant of GaAs and SiGe are close to each other.

For claims 7 and 14, the determination of the thickness of the GaAs layer as claimed would have been obvious to one skilled in the art for the same reason noted above.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang

Trung Dang
Primary Examiner
Art Unit 2823

10/30/05